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Sheet	1	of	1	Attorney Docket Number	29898/41747
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.*	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.*	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		CA 2 448 549	11-28-2002	IPFlex Inc.		✓
		EP 1 416 388	05-06-2004	IPFlex Inc.		✓

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BABB <i>et al.</i> , "The Raw Benchmark Suite: Computation Structures for General Purpose Computing," <i>IEEE J. Comp. Soc.</i> , Sec. 3.1, PP. 134-143 (1997).	
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		CHEN <i>et al.</i> , "An Integrated System for Rapid Prototyping of High Performance Algorithm Specific Data Paths," <i>IEEE Comput. Soc.</i> , pp. 134-148 (1992).	
		COMPTON <i>et al.</i> , "Reconfigurable Computing: A Survey of Systems and Software," <i>ACM Computing Surveys</i> , 34:171-210 (2002).	
		CRONQUIST <i>et al.</i> , "Architecture Design of Reconfigurable Pipelined Datapaths," <i>IEEE Comput. Soc.</i> , Sec. 1 and 2.1, pp. 23-40 (1999).	
		CRONQUIST <i>et al.</i> , "Specifying and Compiling applications for RaPID," <i>IEEE Comput. Soc.</i> , Secs. 3 and 4, pp. 116-125 (1998).	
		HAUSER <i>et al.</i> , "Garp: A MIPS Processor with a Reconfigurable Coprocessor," <i>IEEE Comput. Soc.</i> , pp. 24-33 (1997).	
		MIRSKY <i>et al.</i> , "A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," <i>IEEE Comput. Soc.</i> , Sec. 2.2:157-166 (1996).	
		SINGH <i>et al.</i> , "MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications," <i>IEEE Transactions on Computers</i> , 49:465-474 (2000).	
		Supplementary European Search Report for European patent application No. 04746469.8 - 2224 dated August 10, 2006.	

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